REMARKS/ARGUMENTS

I. THE SECTION 112 REJECTION OF CLAIMS 1-9 SHOULD BE WITHDRAWN

In the Office Action, claims 1-9 are rejected under 35 U.S.C. 112 as failing to comply with the written description requirement and the enablement requirement. According to the Office Action, "[t]he original disclosure does not present a multistage pipeline within the execution unit much less plural instructions from different instruction streams in different stages of a multistage pipeline within the execution unit." Office Action at p. 2, ¶ 1 to p. 3, ¶ 1. As currently amended, claims 1-9 recite a multistage pipeline as follows:

> **"at a given time, the multistage pipeline includes instructions from different ones of the instruction streams in different stages of the multistage pipeline."**

Applicants respectfully submit that the original disclosure of the present application fully describes such a multistage pipeline, in compliance with both the written description requirement and the enablement requirement.

A. The original disclosure of the present application provides written disclosure of the claimed multistage pipeline

To satisfy the written description requirement, a patent disclosure must describe the claimed invention in sufficient detail that one of ordinary skill in the art can reasonably conclude that the inventor had possession of the claimed invention. MPEP § 2163(I). The original disclosure of the present application, which includes the specification, figures, and an appendix, describe specific embodiments of the claimed multistage pipeline in careful detail. For example, under the "Pipelining and Multithreading" section of the specification, Fig. 12 shows a timing diagram for a multistage pipeline that includes instructions from different ones of multiple instruction streams, in different stages of the multistage pipeline[1]:

[1] As shown here, Fig. 12 has been annotated with a downward arrow "↓" to indicate an example of a particular point in time in the multistage pipeline.

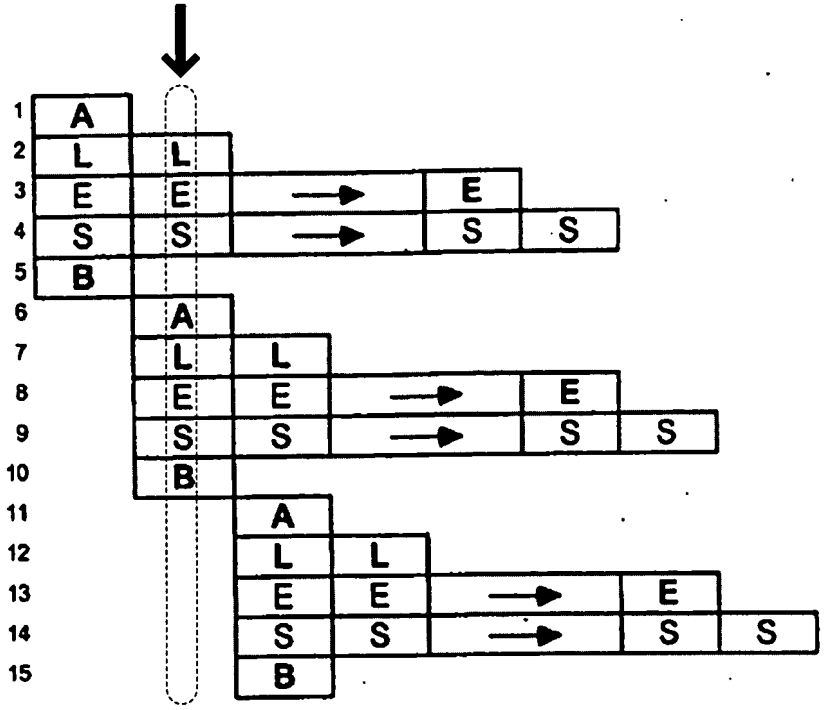

Fig. 12

As shown in this figure, the multistage pipeline contains different instructions. The instructions are labeled as A, L, B, E, and S, which correspond to register-to-register address calculation, memory load, branch, register-to-register data calculation, and memory store instructions. See Specification at ¶ 137. The instructions move through the multistage pipeline in stages, such that a new instruction can begin to be processed before a previous instruction is completed. Also, the instructions may come from instruction streams for two or more independent threads. See Specification at ¶ 138 ("According to one embodiment of the present invention, very highly pipelined implementations are provided by alternating execution of two or more independent threads") and ¶ 139 ("In one embodiment, five simultaneous threads of execution ensure that resources which may be used every two or four cycles are fairly shared by allowing the instructions which use those resources to be issued only on every second or fourth issue slot for that thread").

A downward arrow "↓" has been added to Fig. 12 to indicate a particular point in time in the execution of the multistage pipeline. At this given time, there are numerous instructions in

progress, including a first "E" instruction (row 3) and a second "E" instruction (row 8). Specifically, at the given time indicated by the downward arrow, the first "E" instruction has already completed its first stage of execution and is in the second stage of the multistage pipeline. At the same time, the second "E" instruction has just begun its first stage of execution and is in the first stage of the multistage pipeline. As mentioned previously, instructions such as the first "E" instruction and the second "E" instruction can come from different instruction streams. Clearly, Fig. 12 and corresponding descriptions in the specification illustrate a multistage pipeline that, at a given time, includes instructions from different instruction streams in different stages of the multistage pipeline. Such disclosures unquestionably apprises one of ordinary skill in the art that the inventors were in possession of the claimed invention.

Further evidence that the original disclosure of the present application satisfies the written description requirement for the claimed multistage pipeline is provided by way of a declaration from Mr. Korbin Van Dyke that is included with this Response. In his declaration Mr. Van Dyke states that the execution of instructions as claimed must involve: (1) a multistage pipeline; (2) instructions from a plurality of instruction streams; and (3) at a given time, the multistage pipeline including instructions from different one of the instruction streams in different stages of the multistage pipeline. See Van Dyke declaration, ¶ 18. Mr. Van Dyke further states that, based on the facts set forth in his declaration, it is his opinion that the original disclosure of the present application describes the claimed multistage pipeline in sufficient detail that a person of ordinary skill in the art can readily conclude that the inventors were in possession of the claimed invention. See e.g., Van Dyke declaration at ¶¶ 18-19 and 21-26.

Accordingly, for all of the reasons stated above, Applicants respectfully submit that the description included in the original disclosure of the present application meets the written disclosure requirement of 35 U.S.C. § 112, first paragraph.

B. The original disclosure of the present application enables one of ordinary skill in the art to practice the claimed multistage pipeline

In order to satisfy the enablement requirement, a patent disclosure, when filed, must contain sufficient information regarding the subject matter of the claims as to enable one of ordinary skill in the pertinent art to make and use the claimed invention. MPEP § 2164.01. Whether the enablement requirement is met depends on whether undue experimentation is necessary for one of skill in the art to practice the invention in light of the disclosure. *Id.*

In making the enablement rejection, the Office Action states that the original disclosure "does not provide a description of how plural instructions from different instruction streams would be in different stages of a multiple stage pipeline within the execution unit in a manner where the execution unit could execute the instructions in a properly timed manner. It would require undue experimentation for one of ordinary skill in the DP art to provides [sic] for and perform these limitations." Office Action at p. 3, ¶ 1.

Applicants respectfully disagree. As discussed previously, under the "Pipelining and Multithreading" section of the specification, Fig. 12 shows a timing diagram for a multistage pipeline that includes instructions from different ones of multiple instruction streams, in different stages of the multistage pipeline. The figure illustrates the timing of various A, L, B, E, and S instructions. The figure shows exactly when each instruction would begin and end. The figure also shows the precise timing alignment among the various instructions, down to the level of specific stages. That is, the figure shows exactly how each stage of an instruction would align in time with the stages of other instructions. Thus, the patent disclosure clearly describes how different instructions from different instruction streams would be in different stages of a multistage pipeline, such that the instructions can be executed in a properly timed manner.

One of ordinary skill in the art would not be required to perform undue experimentation – or any experimentation at all for that matter – to understand exactly how to align the different stages of the various instructions so that instructions would be executed in a properly timed manner. This is because the present specification does not leave the timing of execution of the various instructions unspecified. Quite to the contrary, the present specification unambiguously

illustrates in Fig. 12, for example, the precise timing of each stage of the various instructions as they would be executed in the multistage pipeline.

Further evidence that the original patent disclosure provides sufficient information for a person of ordinary skill in the art to both make and use the claimed invention is provided in the declaration of Mr. Korbin Van Dyke included with this Response. Mr. Van Dyke reviewed the original patent disclosure of the present application, including the specification, figures, and appendix, and states that based on his review of these materials, it is his opinion that a person of ordinary skill in the art would have been enabled to make and use, without undue experimentation, the claimed "executing instructions from each instruction stream received at the execution unit in a multistage pipeline within the execution unit such that, at a given time, the multistage pipeline includes instructions from different ones of the instruction streams in different stages of the multistage pipeline." See e.g., Van Dyke declaration at ¶¶ 18-19 and 21-26.

In fact, Mr. Van Dyke notes with particular emphasis that the level of clarity and detail presented in the appendix (referred to in Mr. Van Dyke's declaration as the "Zeus manual") undoubtedly enables one of ordinary skill in the art to make and use the claimed invention. Mr. Van Dyke states, at ¶ 30 of his declaration:

> **"During my evaluation of the media processor patent application, I have been impressed by the thoroughness and overall high-quality of the Zeus manual. The manual provides clear and unambiguous descriptions of media processing systems and is thorough and well-written. The information in the manual would have been readily understood and easily accessible to software engineers coding the media processing systems, and hardware engineers implementing microprocessors for use in the media processing systems, and that is exactly what an architecture reference manual should be. This is not surprising, since the 10/757,515 patent application includes an architecture manual that is intended to be used by hardware engineers to do exactly that – design, build, and implement a media processor that would include circuitry for 'executing instructions from each instruction stream received at the execution unit in a multistage pipeline such that, at a given time, the multistage pipeline includes instructions from different ones of the instruction streams in different stages of the multistage pipeline' as described in the Zeus architecture manual."**

For all of the reasons discussed above, Applicants respectfully submit that the original disclosure of the present application meets the enablement requirement of 35 U.S.C. § 112, first

paragraph.

II. CLAIMS 1-4 AND 6-9 ARE PATENTABLE OVER ITO

In the Office Action, claims 1-4 and 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,742,782 issued to Ito et al. ("Ito"). Claims 1 and 4 have been amended to more clearly set forth the distinction between the present invention and the cited reference Ito and to improve readability. As amended, claims 1 and 4 and their respective dependent claims are patentable over Ito.

Claim 1

As amended, claim 1 recites:

> **"a single instruction that specifies an operation to cause multiple instances of the operation to be performed, each instance of the operation to be performed using a different one of the plurality of data elements in partitioned fields of the at least one register to produce a catenated result" (emphasis added)**

The amended claim language of claim 1 requires that a single instruction specify an operation to cause multiple instances of the operation to be performed, each instance to be performed using a different one of the plurality of data elements in partitioned fields of at least one register. For example, in one embodiment of the invention, a "Group Add" instruction is carried out with a 128-bit register that contains sixteen individual 8-bit operands in partitioned fields. That is, the "Group Add" instruction specifies an ADD operation, and sixteen instances of the ADD operation are performed, each instance being performed on one of the sixteen individual 8-bit operands. Accordingly, sixteen different individual add operations may take place as the result of a single "Group Add" instruction. See specification at 0221.

By contrast, Ito discloses a very long instruction word (VLIW) instruction that specifies four operations, each to be performed in a traditional manner. That is, only one instance of each operation is to be performed. Fig. 8 of Ito illustrates the VLIW format:

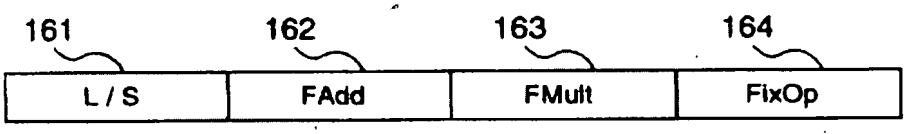

Fig. 8 of Ito

As seen in this figure, the VLIW format contains four different operations: (1) a load/store (L/S) operation, (2) a floating-point add (FAdd) operation, (3) a floating-point multiply (FMult) operation, and (4) a fixed-point operation (FixOp). Each of these four operations is performed only once. In a sense, Ito merely teaches that four conventional instructions can be specified together, using the "very long" format. Nowhere in the disclosure of Ito is there any teaching or even remote suggestion that an operation can be specified to cause multiple instances of the operation to be performed.

In fact, Ito actually teaches away from the invention as recited in claim 1. To perform one instance of an operation, Ito requires that the operation be specified in a VLIW instruction. To perform another instance of the same operation, Ito requires the operation be specified again in a VLIW instruction. Thus, to perform sixteen different instances of an ADD operation, for example, Ito would require the ADD operation to be specified sixteen separate times. This is the antithesis of a single instruction that specifies an operation to cause multiple instances of the operation to be performed, each instance of the operation to be performed using a different one of the plurality of data elements, as recited in claim 1. Accordingly, Applicants respectfully submit that claim 1 is patentable over Ito.

Claims 2-4

Claims 2-4 depend from claim 1 and therefore incorporate all of its limitations. For at least the reasons discussed above with respect to claim 1, claims 2-5 are patentable over Ito.

Furthermore, claim 2 is patentable over Ito for the additional reason that Ito fails to disclose "wherein the number of threads executing within the execution unit is prime relative to a rate of execution of a slowest functional unit in the execution unit," as recited in claim 2. The Office Action merely states that in Ito, "the number or threads is three (A, B, C), which is a

prime number." Office Action at p. 5, ¶ 2. However, claim 2 does not just require that the number of threads executing within the execution unit be a prime number. Instead, claim 2 requires that the number of threads executing within the execution unit be prime relative to the rate of execution of a slowest functional unit in the execution unit. The Office Action does not point to any portion of Ito that teaches or suggests such a claimed feature. For at least this additional reason, claim 2 is patentable over Ito.

Claim 6

Claim 6 is rejected based on the same rationale as claim 1. For at least similar reasons as stated above with respect to claim 1, claim 6 is patentable over Ito.

Claims 7-9

Claims 7-9 depend from claim 6 and therefore incorporate all of its limitations. For at least the reasons discussed above with respect to claim 6, claims 7-9 are patentable over Ito.

Furthermore, claim 7 is rejected based on the same rationale as claim 2. For the additional reason stated above with regard to claim 2, claim 7 is patentable over Ito.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (202) 756-8000.

Respectfully submitted,
McDERMOTT WILL & EMERY LLP

Demetria A. Buncum
Registration No. 58,848

600 13th Street NW
Washington, DC 20005-3096
Phone: 202.756.8000 DAB
Facsimile: 202.756.8087
Date: May 29, 2007

Please recognize our Customer No. 20277 as our correspondence address.